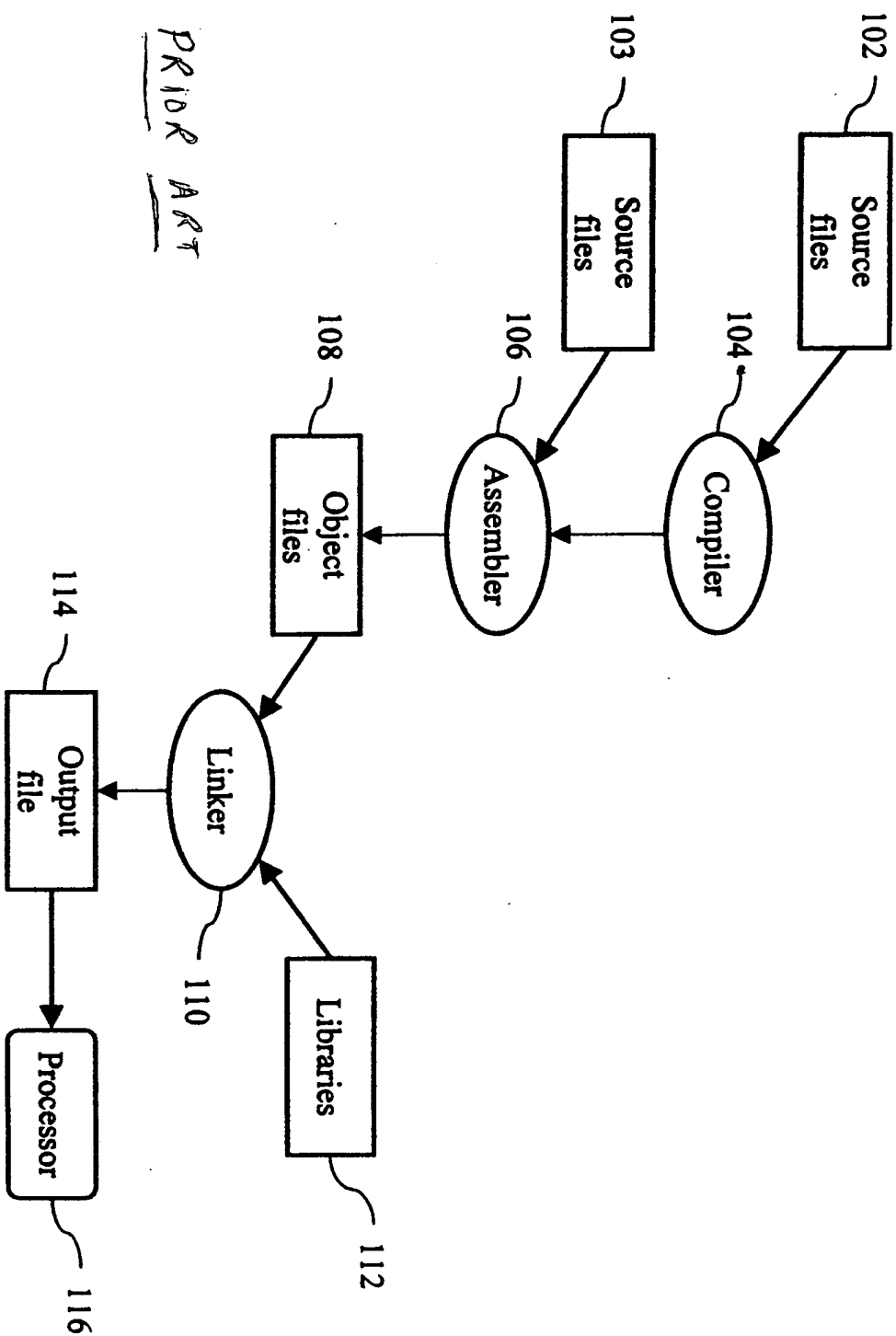


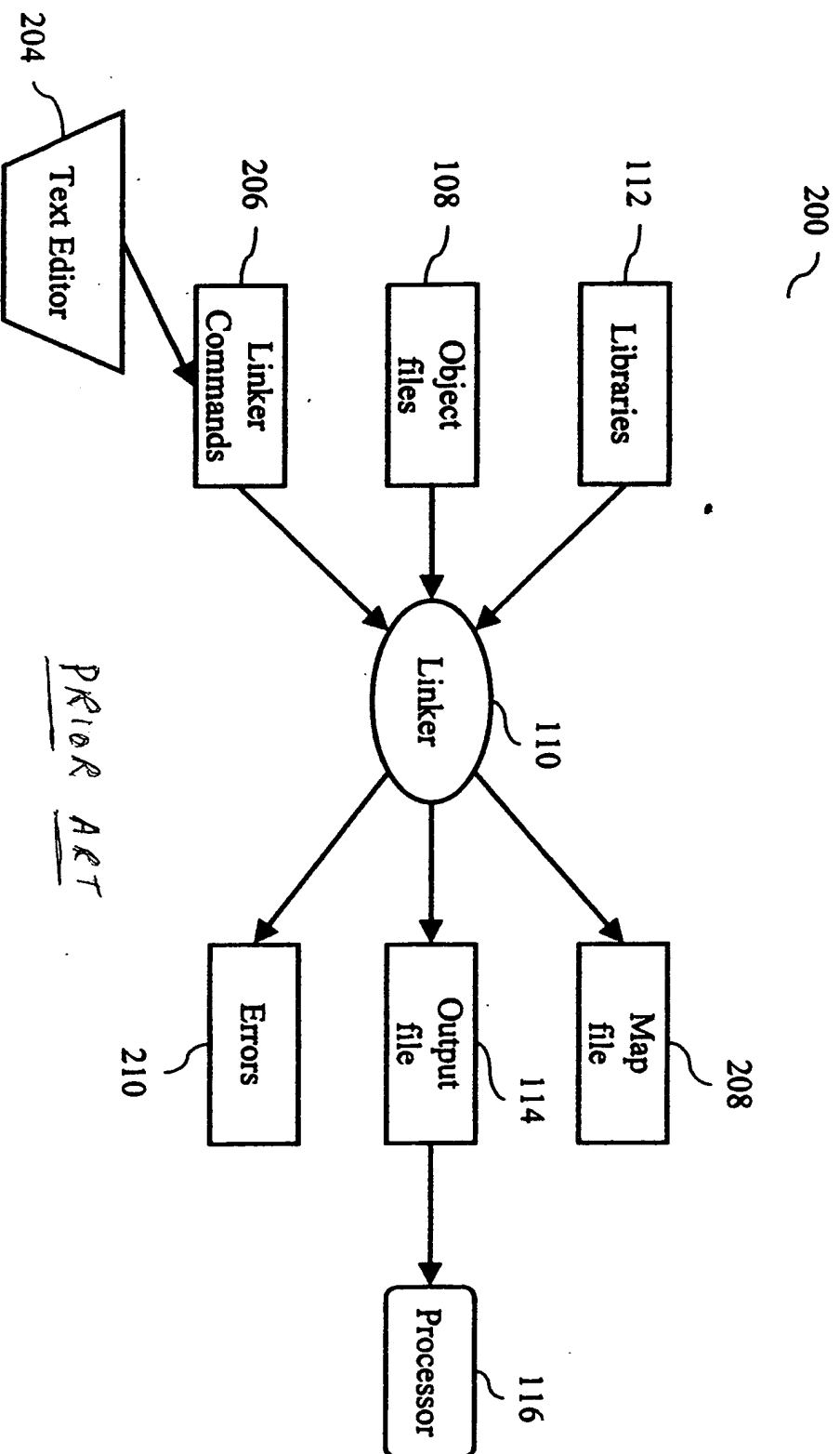
Figure 1: Development Flow



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Figure 2A: Typical Linker Apparatus



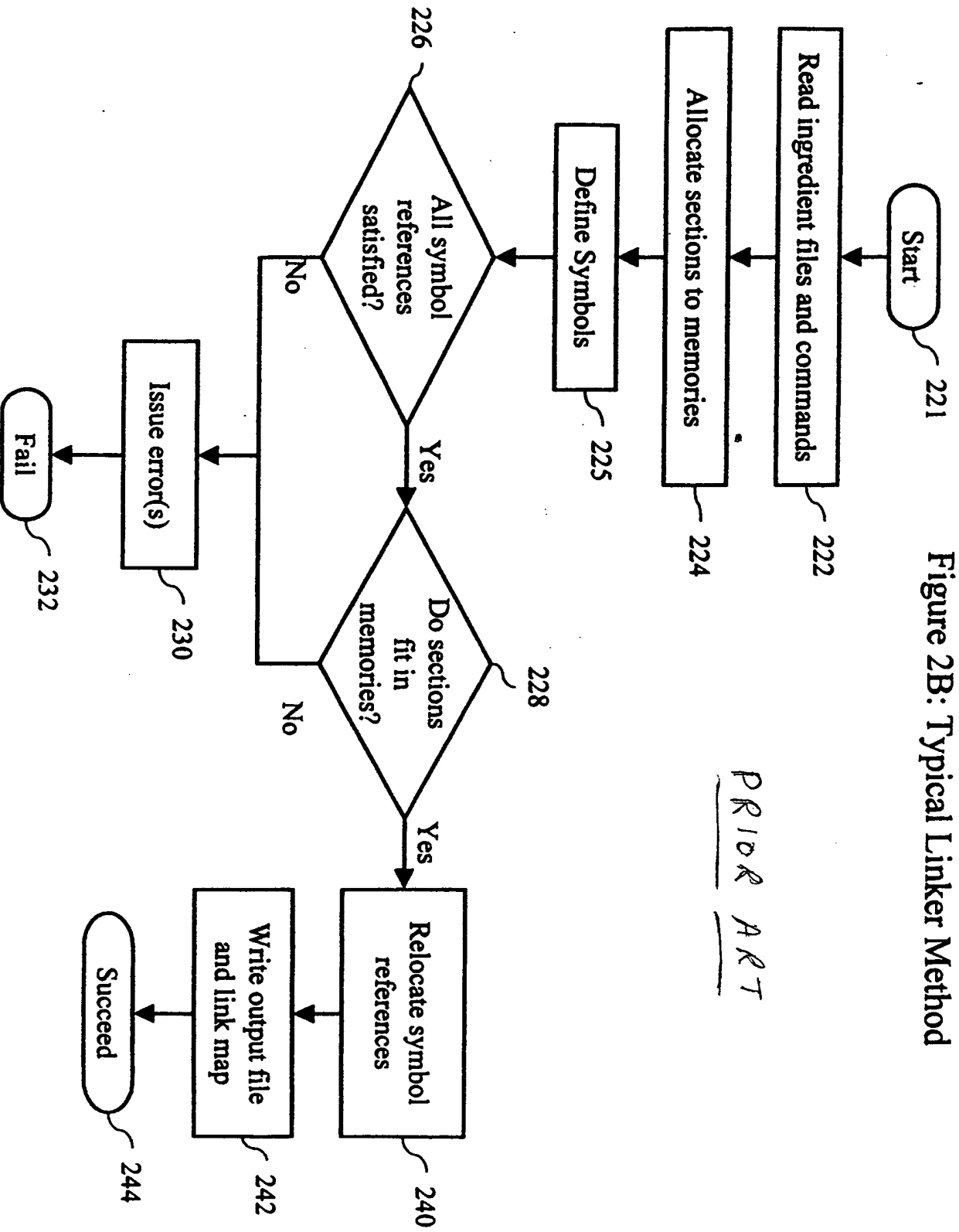


Figure 3: Linker Allocation and Output

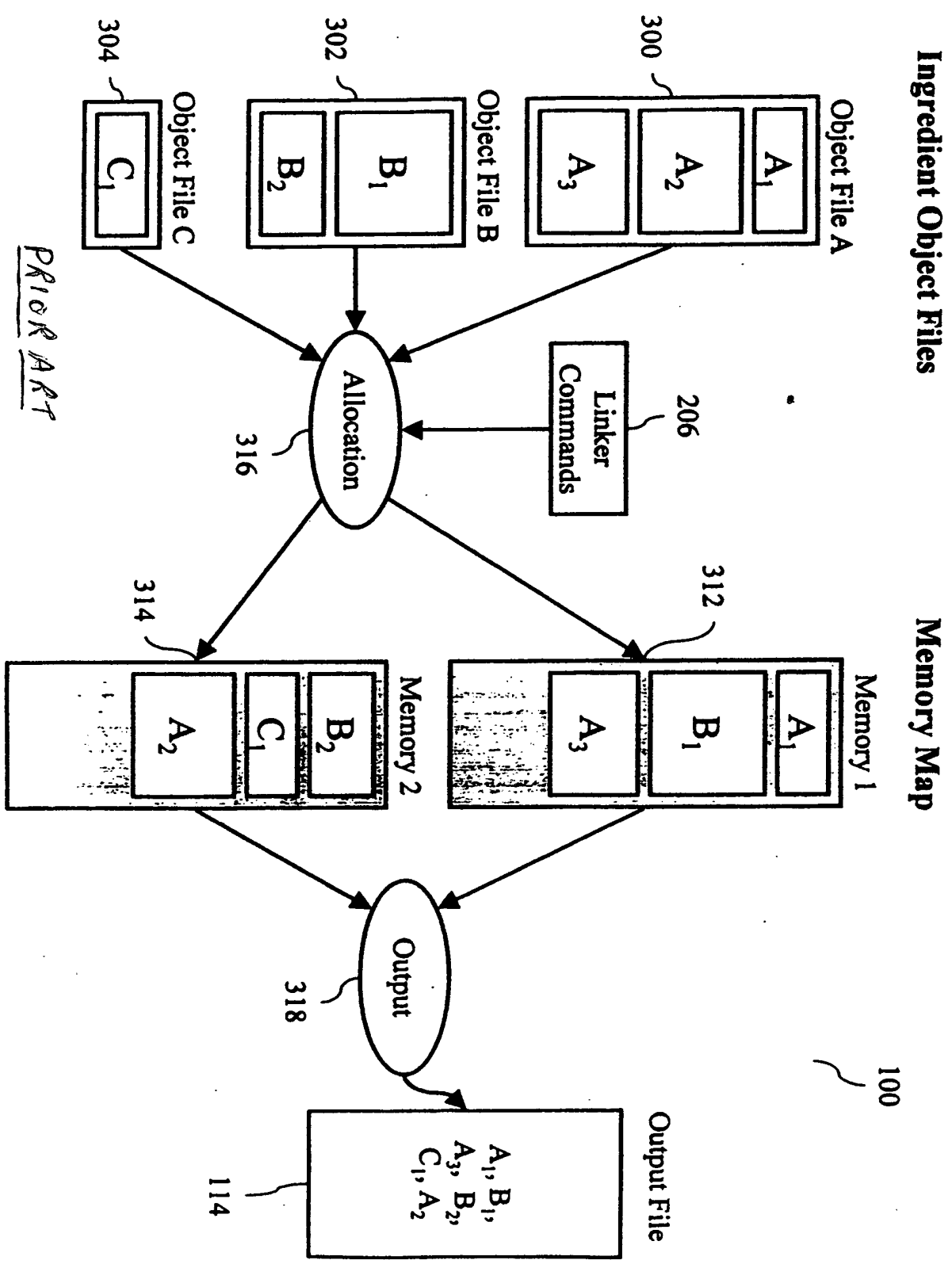


Figure 4: Linker Symbol Resolution

